Self-Timed Control of Multiphase Switched Capacitor Converters

Sergey Mileiko[†], Alexander Kushnerov[‡], Danil Sokolov[†], Alex Yakovlev[†]
[†]Newcastle University, UK; [‡]National Cheng-Kung University, Taiwan

***Abstract*—The paper proposes a method to synthesize a digital controller for multiphase switched capacitor converters (SCCs). A specific requirement to the controller is that, regardless of external conditions, it should provide pulses of fixed frequency and width. Asynchronous (self-timed) digital circuits fulfil this requirement by definition. However, their design can be quite complex, especially if an SCC has a large number of switches. The paper shows how, based only on observations and simple rules, one can use an existing CAD tool to synthesize, verify and fit to available library components a circuit of self-timed controller. The simulations demonstrate the operation of the controller designed using the proposed method.**

I. Introduction

Switched capacitor converters (SCCs) are favored in some applications due to low EMI and compatibility with integrated circuit technology. One of the biggest disadvantages of the SCCs is their efficient operation only in a certain number of target voltages. These voltages are defined by the ratios of the SCC. The voltages beyond the target can also be generated, but only at the expense of the efficiency reduction. To avoid an essential efficiency reduction, the converters with large number of ratios are used. The state of the art solution is the multiphase SCC with binary resolution [1]. This type of converters can provide $2^N - 1$ ratios, where N is the number of flying capacitors. Fig. 1 shows the schematics of a simple step-down multiphase converter with $N = 2$ flying capacitors.

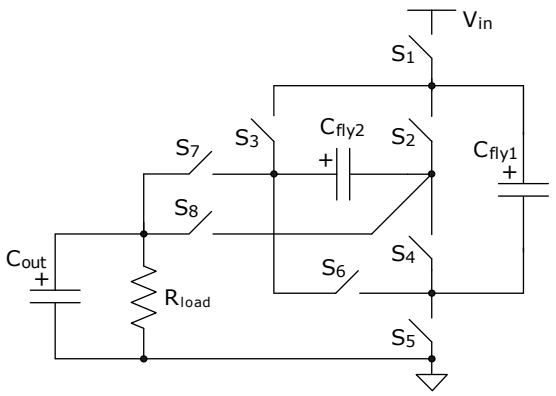

Fig. 1. Schematic of the multiphase SCC with two flying capacitors.

The converter has $4 \times N$ switches that allow to set special topologies of the flying capacitors to provide a certain ratio of the converter. The task of controlling these switches is not trivial, and can become quite complicated with higher N.

Requirements for the switches' controller are as follows:

- Oscillate among several predefined topologies for each specific ratio.
- Control the delay between phases (switching frequency).
- Provide a dead-time between phases to prevent the shoot-through currents [2].
- Prevent the errors during the ratio change (when the ratio is changed at the same time with an internal signal).

The most of these requirements can be supported by the self-timed controller designed in [2]. However, this method is specified only for the two-phase SCC, and it does not consider the case with additional inputs defining the converter's ratio. In this paper we expand the method of designing the self-oscillating controllers, presented in [2],for the case of multi-phase SCC. The method allows to systematize the process of the design of the SCC control. A simple algorithm based on this method can be generated. The inputs to the algorithm will be the states of the switches in each topology, and its output - a self-timed circuit of the SCC controller.

A self-timed controller simplifies the design of the SCC, because it does not need a clock signal, which sometimes can be complicated to deliver and adjust. Moreover, such a controller does not consume any dynamic power in a stand-by mode, as there is no clock signal to oscillate.

II. Proposed approach

Table I shows all the topologies for different ratios of the SCC in Fig. 1. These topologies are alternating in 3 phases for the ratios $1/4$ and $3/4$, and in 2 phases for the ratio $2/4$. The value $'1'$ in the table indicates that the corresponding switch is turned on, and the value $'0'$ – is turned off.

The high-level schematic of the SCC controller is shown in Fig. 2. The controller block operates the switches of the SCC with signals $S1 - S8$. The number of external delay elements is equal to the largest number of phases (i.e. $N + 1$). For the ratios $1/4$ and $3/4$ there are 3 phases, so we use 3 delay

TABLE I
Specification of the topologies.

Ratio	Phase	S1	S2	S3	S4	S5	S6	S7	S8
$\frac{1}{4}$	1	1	0	0	0	0	1	0	1
	2	0	0	1	0	1	0	0	1
	3	0	0	0	1	1	0	1	0
$\frac{2}{4}$	1	1	0	1	1	0	0	0	1
	2	0	0	1	1	1	0	1	0
$\frac{3}{4}$	1	0	1	0	0	1	0	1	0
	2	1	0	0	1	0	0	1	0
	3	1	0	1	0	0	0	0	1

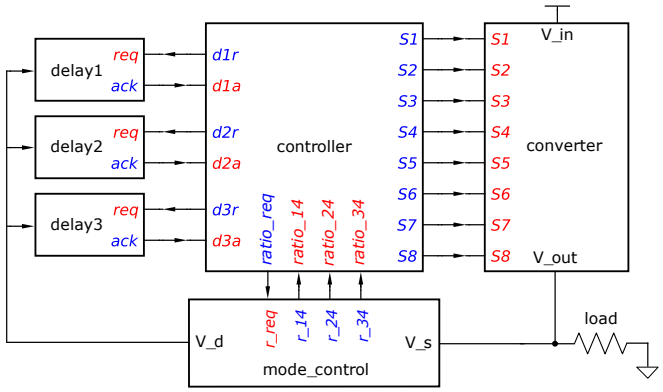

Fig. 2. Interface of SCC controller.

elements. Each delay element provides two time intervals: one for the phase delay, and another for the dead time delay. Communication with the delay elements is implemented by two signals: The delay request ($d1r$, $d2r$, $d3r$) is sent from the controller to the delay element, and after the delay the controller receives an acknowledgement ($d1a$, $d2a$, $d3a$).

The mode_control block specifies the ratio of the SCC with signals $ratio\_14$, $ratio\_24$, and $ratio\_34$. These signals are operating in one-hot mode. The ratio can be changed at any time, and if a ratio signal arrives at the same time with the change of an internal signal, it may result in metastability in the system, or even in the wrong outputs. To prevent these errors the ratio request $ratio\_req$ is introduced. It allows to change the ratio only when there is no switching in the controller. The mode_control block must set the ratio only when $ratio\_req$ is high. The controller block sends the ratio request at the end of every cycle, and starts the new cycle only after the ratio is set.

The mode control block provides the feedback of the converter. It measures the output voltage with its sensor input (V_s), chooses the converter's ratio, and controls the delay elements with its output V_d. The design of this block depends on the application of the converter, and is not considered in this paper. Examples of SCC feedback can be found in [3]. The main focus of this paper is the controller block.

To specify the behavior of the SCC controller formally, we use Signal Transition Graphs (STG) [4]. In the following this will allow us to synthesize its circuit automatically using the Workcraft environment [5]. STG is a special type of Petri nets whose transitions are associated with the rising and falling edges of signals (denoted by "$+$" and "$-$" after the signal name). Causality between the signal events is captured by means of directed arcs. Tokens (dots on the arcs) define the initial states. For the sake of convenience, the input signals are highlighted by red, the output signals - by blue, and the internal signals - by green.

The first step of the controller design is defining STG specification for each ratio, obeying the following rules:

- In the initial state all the switches are turned off (switch control signals are $'0'$), and all the signals between the controller and the delay elements (delay requests and acknowledgements) are equal to $'1'$.
- The switching sequence of an i delay element must be following: $dir-$, $dia-$, $dir+$, $dia+$.
- The switching starts with resetting the first delay request (signal $d1r$), and ends with setting the last delay acknowledgement (signal $d3a$ in the example case). For the ratios with the smaller number of phases the delays before the last are skipped. In the example, for the ratio $1/2$ the delay 1 is followed by the delay 3, and the delay 2 is skipped.
- The switches of a certain topology must be turned on after the reset of the delay requests, and turned off after the set of the delay request.
- The switches, which remain on in several topologies in a row, do not turn off between these topologies.

The example of STG for the ratio $1/4$ is shown in Fig. 3. The arcs from delay requests to delay acknowledgements in this STG can be removed because of the transitivity property, however they do not affect the STG, and are left for better visual representation. The timing diagrams depicted in Fig. 4 demonstrate the causality links between the signals in the STG.

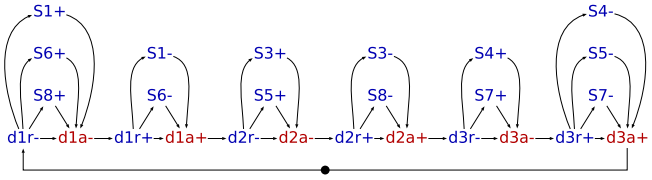

Fig. 3. Formal STG specification for 1/4 ratio control.

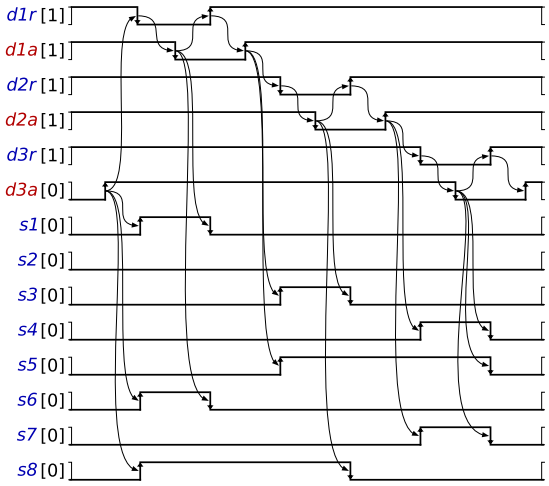

Fig. 4. Informal timing diagram for 1/4 ratio switching.

The next step is to design an STG of the part of the controller that chooses the ratio and communicates with an environment. This STG for the example SCC is shown in Fig. 5. The initial state is marked by places with tokens. The first transition is sending the ratio request (switching the signal $ratio\_r$ to $'1'$). After that, the environment is allowed to send the ratio to the controller. When the ratio arrives, the controller

starts the first phase of a chosen ratio by resetting the first delay request, as it was described above. At the same time it allows to reset the ratio signal from the environment. When the acknowledge signal of the last phase arrives, the system turns all the switches off, and sends the new ratio request.

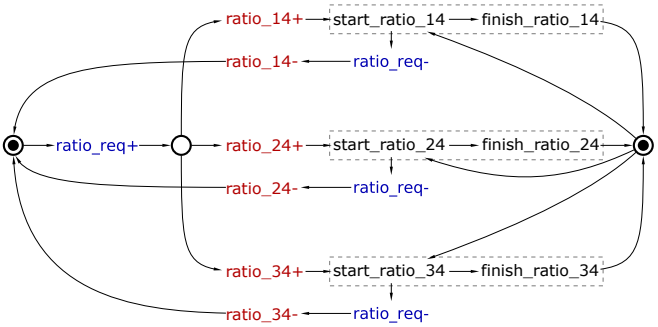

Fig. 5. STG specification of multiphase SCC controller.

The STG contains the arcs that lead to the input signals. The controller cannot control its inputs, because the inputs are specified by the environment that is external for the controller. However, we can assume the behavior of the environment. These assumptions are stated below.

- The environment sends only one ratio signal, and only when it is requested. This ratio signal resets right after the request is reset.
- The ratio signal resets before the delay acknowledgment arrives. This assumption means that delay, provided by the delay element takes more time than the communication between the controller and the environment. This assumption is not necessary, however, the circuit can become more complicated without it.
- The delay acknowledgement signals arrive later than the switch control signals change their value.

The delay element provides two delays: the phase delay for the transition from $'1'$ to $'0'$, and the dead time delay for the transition from $'0'$ to $'1'$. One of the possible implementations of such delay could be connecting the outputs of both delay elements to an OR gate.Because the phase delay is always greater than the dead time delay, the duration of transition from $'1'$ to $'0'$ would be equal to the phase delay, and from $'0'$ to $'1'$ - to the dead time delay.

Since the dead time delay is short, it can be implemented as a chain of inverters. In step-down SCCs, where the power stage is built on transmission gates, Vdd of the controller can be used as a bias for the substrates of power p-MOS transistors. In this case, change in Vdd will cause change in the delay of switches and in the delay of inverters. These changes will occur in the same direction that should contribute to avoiding the shoot-through currents. The phase delay is much longer than the dead time delay and requires more sophisticated solutions. This solution can be a leakage-based delay element [6]. Some other techniques to realize long delays can be found in [7], [8]. However, this element must specify the following requirement: its delay of $'1'$ must be not larger than the delay of $'0'$. Otherwise, it may not set to $'1'$, when the new $'0'$ arrives.

III. Simulation results

The STG designed in the previous section has been transformed into a circuit using the Pertify tool [9] from the Workcraft environment. The generated circuit is built of the gates from the libraries of the technology AMS350nm. Such technology has lower static losses comparing to dynamic ones. That allows to estimate the dynamic losses of the asynchronous controller. The generated controller circuit has 372 transistors. The controller has been simulated in the Cadence Analog Design Environment tool. To simplify the simulation, the virtual delay elements are used to implement the dead time and the phase delays.

Since the main focus of this paper is in the controller, the mode control block is simplified in the simulations. There is no feedback from the converter, and the delays are constant. In the current simulations the phase delay is $1\mu s$, and the dead time delay is $1ns$. The resulting switching frequency is approximately equal to $1MHz$. The ratios are the inputs of the simulated circuit. However, the interface of the controller requires the ratio signals to be equal to $'1'$ only when the ratio request arrives. To satisfy this requirement, each ratio input goes through an AND gate with the $ratio\_req$ signal.

The converter circuit is the same as in Fig. 1. Its parameters are the following: $C_{fly1} = 200pF$, $C_{fly2} = 100pF$, $C_{out} = 600pF$, $R_{load} = 1M\Omega$. The switches have been designed as transmission gates with the pmos $30\mu m$ width and the nmos $10\mu m$ width. The structure of the switches is the same as in [2]. The input and supply voltages V_{in} and V_{dd} are equal to $3.3V$.

To demonstrate the operation of the SCC, it has been set in series to the ratios $1/4$, $2/4$, $3/4$ and $1/4$. The expected values of V_{out} are $0.825V$, $1.65V$, $2.475V$ and $0.825V$ respectively.

The results of the simulation are shown in Fig. 6. When the requested ratio was set to $1/4$, the output voltage became $0.82V$. Then, after changing the ratio to $2/4$, the voltage changed to $1.64V$. When the ratio was set to $3/4$, the voltage became $2.46V$. Afterwards, when the ratio was set back to $1/4$, the voltage returned to $0.82V$. A high degree of inertia of the output voltage is due to the relatively high output capacitance and large load resistance.

The signal $ratio\_req$ was periodically sent to the mode control block, but most of the time it was $'0'$. In the end of the simulation, when there were no ratio signals, it has remained in $'1'$, waiting for the next ratio signal arrives.

The control signals to the switches $(S1 - S8)$ were sent according to the specification of the topologies from Table I. The phase period was $1\mu s$ as it was set to the phase delay element. The dead time was around $2ns$ - the delay of the logic gates has been added to the delay.

Fig. 7 shows the power of the controller in different operation modes. Although, for all the ratios the power consumption grows linearly with frequency increase, in a stand-by mode the controller does not consume any dynamic power.

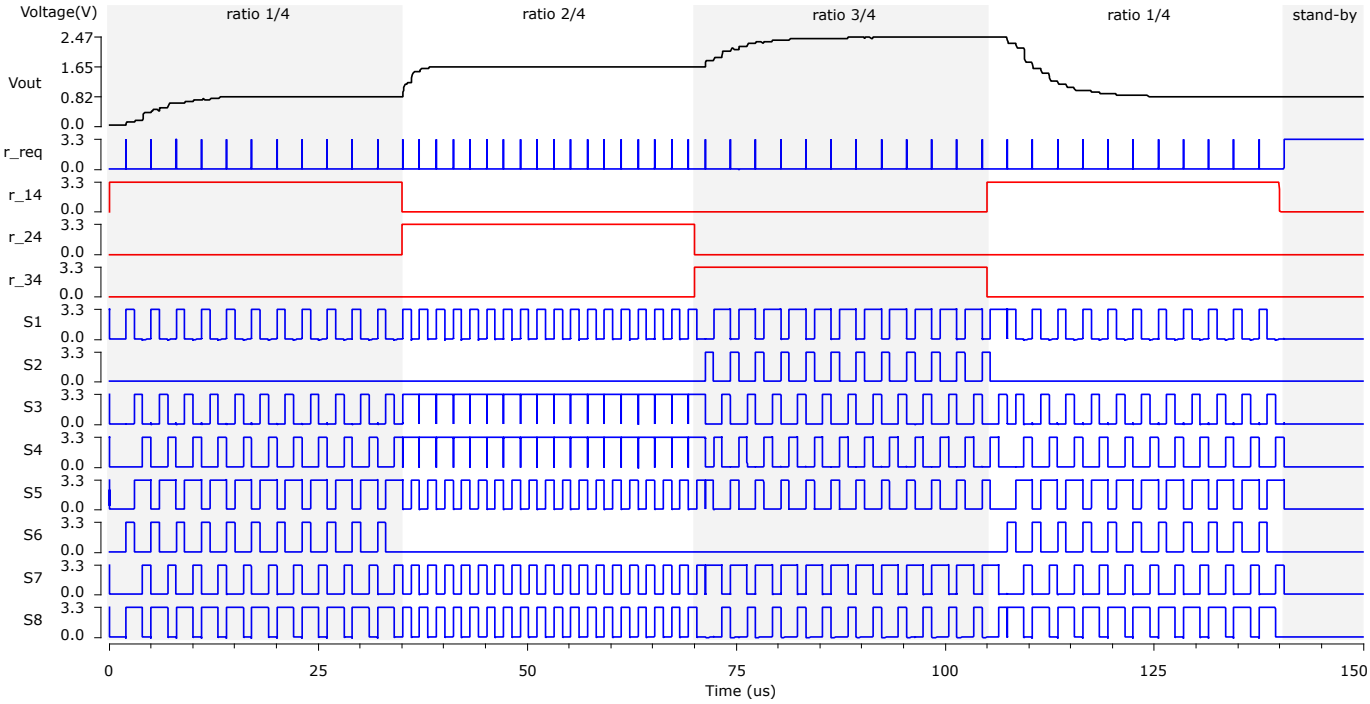

Fig. 6. Simulation results.

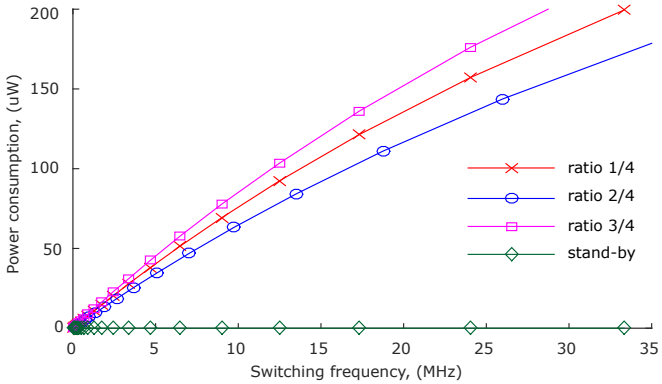

Fig. 7. Power consumption of the SCC controller

IV. Conclusion and Discussions

The proposed method allows designing self-timed controllers for SCC. The steps described in Section II can be automated. Ideally, a user would have to input only the required ratios and topologies of a designed SCC, and an algorithm based on this method would produce a completed implementation of the corresponding controller.

The dead time delay is usually rather small: it is comparable to the delay of a logic gate and is three orders of magnitude smaller than a phase delay. Therefore inaccuracy in this delay caused by the process variation would not have a critical affect on the efficiency of the entire system.

While the generated controller is quite large, its size can be reduced. One of the possible ways of doing this is by using the David cells [10] in the controller part that interfaces the delay elements. Another optimization is to simplify the operation of the signal $ratio\_req$ in such a way that it does not interrupt the generation of the switch control signals. These optimization possibilities are a subject for future research.

Acknowledgement

This research was supported by EPSRC, grants SAVVIE (EP/K012908/1) and A4A (EP/L025507/1).

References

[1] A. Kushnerov and S. Ben-Yaakov, "Unified algebraic synthesis of generalised Fibonacci switched capacitor converters," *IET Power Electronics*, vol. 7, no. 3, pp. 540–544, 2014.

[2] S. Mileiko, A. Kushnerov, D. Sokolov, and A. Yakovlev, "Self-timed control of two-phase switched capacitor converters," in *International Conference on the Science of Electrical Engineering (ICSEE)*, 2016.

[3] T. V. Breussegem and M. Steyaert, "Cmos integrated capacitive dc-dc converters." Springer, 2013.

[4] L. Rosenblum and A. Yakovlev, "Signal graphs: from self-timed to timed ones," in *IEEE int. Workshop on Timed Petri Nets*, 1985.

[5] D. Sokolov, V. Khomenko, and A. Mokhov, "Workcraft: Ten years later," in *This asynchronous world. Essays dedicated to Alex Yakovlev on the occasion of his 60th birthday*, A. Mokhov, Ed. Newcastle University, 2016, available online http://async.org.uk/ay-festschrift/paper25-Alex-Festschrift.pdf.

[6] W. Jung, S. Oh, S. Band, Y. Lee, Z. Foo, G. Kim, Y. Zhang, D. Sylvester, and D. Blaauw, "An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, 2014.

[7] G. Kim, M.-K. Kim, B.-S. Chang, and W. Kim, "A low-voltage, low-power cmos delay element," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 7, pp. 966–971, 1996.

[8] C.-Y. Yu, C.-C. Chung, C.-J. Yu, and C.-Y. Lee, "A low-power dco using interlaced hysteresis delay cells," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 10, pp. 673–677, 2012.

[9] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev, "Logic synthesis for asynchronous controllers and interfaces," in *Springer*, 2002.

[10] R. David, "Modular design of asynchronous circuits dened by graphs," *IEEE Transactions on Computers*, vol. 26, no. 8, pp. 727–737, 1977.